

## WHAT IS CLAIMED IS:

1. An M-bit adder capable of receiving a first M-bit  
2 argument, a second M-bit argument, and a carry-in (CI) bit  
3 comprising:

4 M adder cells arranged in R rows, wherein a least  
5 significant adder cell in a first one of said rows of adder cells  
6 receives a first data bit,  $A_x$ , from said first M-bit argument and  
7 a first data bit,  $B_x$ , from said second M-bit argument, and  
8 generates a first conditional carry-out bit,  $C_x(1)$ , and a second  
9 conditional carry-out bit,  $C_x(0)$ , wherein said  $C_x(1)$  bit is  
10 calculated assuming a row carry-out bit from a second row of adder  
11 cells preceding said first row is a 1 and said  $C_x(0)$  bit is  
12 calculated assuming said row carry-out bit from said second row is  
13 a 0.

1 2. The M-bit adder as set forth in Claim 1 wherein said  
3 least significant adder cell generates a first conditional sum bit,  
 $S_x(1)$ , and a second conditional sum bit,  $S_x(0)$ .

1 *1st* 3. The M-bit adder as set forth in Claim 2 wherein said  
2  $S_x(1)$  bit is calculated assuming said row carry-out bit from said  
3 second row is a 1 and said  $S_x(0)$  bit is calculated assuming said  
4 row carry-out bit from said second row is a 0.

1 4. The M-bit adder as set forth in Claim 3 wherein said row  
2 carry-out bit selects one of said  $S_x(1)$  bit and said  $S_x(0)$  bit to  
3 be output by said least significant adder cell.

1 5. The M-bit adder as set forth in Claim 4 wherein said  
2 first row of adder cells further comprises a second adder cell  
3 coupled to said least significant adder cell, wherein said second  
4 adder cell receives a second data bit,  $A_{x+1}$ , from said first M-bit  
5 argument and a second data bit,  $B_{x+1}$ , from said second M-bit  
6 argument, and receives from said least significant adder cell said  
7  $C_x(1)$  bit and said  $C_x(0)$  bit.

1 *Jul 19* 6. The M-bit adder as set forth in Claim 5 wherein said  
2 second adder cell generates a first conditional carry-out bit,  
3  $C_{x+1}(1)$ , wherein said  $C_{x+1}(1)$  bit is generated from said  $A_{x+1}$  data bit,  
4 said  $B_{x+1}$  data bit, and said  $C_x(1)$  bit from said least significant  
5 adder cell.

1 7. The M-bit adder as set forth in Claim 6 wherein said  
2 second adder cell generates a second conditional carry-out bit,  
3  $C_{x+1}(0)$ , wherein said  $C_{x+1}(0)$  bit is generated from said  $A_{x+1}$  data bit,  
4 said  $B_{x+1}$  data bit, and said  $C_x(0)$  bit from said least significant  
5 adder cell.

1 8. The M-bit adder as set forth in Claim 7 wherein said  
2 second adder cell generates a first conditional sum bit,  $S_{x+1}(1)$ ,  
3 wherein said  $S_{x+1}(1)$  bit is generated from said  $A_{x+1}$  data bit, said  
4  $B_{x+1}$  data bit, and said  $C_x(1)$  bit from said least significant adder  
5 cell.

1 *John A.* 9. The M-bit adder as set forth in Claim 8 wherein said  
2 second adder cell generates a second conditional sum bit,  $S_{x+1}(0)$ ,  
3 wherein said  $S_{x+1}(0)$  bit is generated from said  $A_{x+1}$  data bit, said  
4  $B_{x+1}$  data bit, and said  $C_x(0)$  bit from said least significant adder  
5 cell.

1 *John A.* 10. The M-bit adder as set forth in Claim 9 wherein said row  
2 carry-out bit selects one of said  $S_{x+1}(1)$  bit and said  $S_{x+1}(0)$  bit to  
3 be output by said second adder cell.

1 *John A.* 11. The M-bit adder as set forth in Claim 1 wherein said  
2 first row of adder cells contains N adder cells and said second row  
3 of adder cells preceding said first row contains less than N adder  
4 cells.

1 *Subj. Pat.* 12. A data processor comprising:  
2 an instruction execution pipeline comprising N processing  
3 stages, each of said N processing stages capable of performing one  
4 of a plurality of execution steps associated with a pending  
5 instruction being executed by said instruction execution pipeline,  
6 wherein at least one of said N processing stages comprises an M-bit  
7 adder capable of receiving a first M-bit argument, a second M-bit  
8 argument, and a carry-in (CI) bit, said M-bit adder comprising:  
9 M adder cells arranged in R rows, wherein a least  
10 significant adder cell in a first one of said rows of adder  
11 cells receives a first data bit,  $A_x$ , from said first M-bit  
12 argument and a first data bit,  $B_x$ , from said second M-bit  
13 argument, and generates a first conditional carry-out bit,  
14  $C_x(1)$ , and a second conditional carry-out bit,  $C_x(0)$ , wherein  
15 said  $C_x(1)$  bit is calculated assuming a row carry-out bit from  
16 a second row of adder cells preceding said first row is a 1  
17 and said  $C_x(0)$  bit is calculated assuming said row carry-out  
18 bit from said second row is a 0.

1 *cancel* 13. The data processor as set forth in Claim 12 wherein said  
2 least significant adder cell generates a first conditional sum bit,  
3  $S_x(1)$ , and a second conditional sum bit,  $S_x(0)$ .

1 14. The data processor as set forth in Claim 13 wherein said  
2  $S_x(1)$  bit is calculated assuming said row carry-out bit from said  
3 second row is a 1 and said  $S_x(0)$  bit is calculated assuming said  
4 row carry-out bit from said second row is a 0.

1 15. The data processor as set forth in Claim 14 wherein said  
2 row carry-out bit selects one of said  $S_x(1)$  bit and said  $S_x(0)$  bit  
3 to be output by said least significant adder cell.

1 16. The data processor as set forth in Claim 15 wherein said  
2 first row of adder cells further comprises a second adder cell  
3 coupled to said least significant adder cell, wherein said second  
4 adder cell receives a second data bit,  $A_{x+1}$ , from said first M-bit  
5 argument and a second data bit,  $B_{x+1}$ , from said second M-bit  
6 argument, and receives from said least significant adder cell said  
7  $C_x(1)$  bit and said  $C_x(0)$  bit.

1 *Sub A1* 17. The data processor as set forth in Claim 16 wherein said  
2 second adder cell generates a first conditional carry-out bit,  
3  $C_{x+1}(1)$ , wherein said  $C_{x+1}(1)$  bit is generated from said  $A_{x+1}$  data bit,  
4 said  $B_{x+1}$  data bit, and said  $C_x(1)$  bit from said least significant  
5 adder cell.

1 18. The data processor as set forth in Claim 17 wherein said  
2 second adder cell generates a second conditional carry-out bit,  
3  $C_{x+1}(0)$ , wherein said  $C_{x+1}(0)$  bit is generated from said  $A_{x+1}$  data bit,  
4 said  $B_{x+1}$  data bit, and said  $C_x(0)$  bit from said least significant  
5 adder cell.

1 19. The data processor as set forth in Claim 18 wherein said  
2 second adder cell generates a first conditional sum bit,  $S_{x+1}(1)$ ,  
3 wherein said  $S_{x+1}(1)$  bit is generated from said  $A_{x+1}$  data bit, said  
4  $B_{x+1}$  data bit, and said  $C_x(1)$  bit from said least significant adder  
5 cell.

1 *final* 20. The data processor as set forth in Claim 19 wherein said  
2 second adder cell generates a second conditional sum bit,  $S_{x+1}(0)$ ,  
3 wherein said  $S_{x+1}(0)$  bit is generated from said  $A_{x+1}$  data bit, said  
4  $B_{x+1}$  data bit, and said  $C_x(0)$  bit from said least significant adder  
5 cell.

1 21. The data processor as set forth in Claim 20 wherein said  
2 row carry-out bit selects one of said  $S_{x+1}(1)$  bit and said  $S_{x+1}(0)$   
3 bit to be output by said second adder cell.

1 22. The data processor as set forth in Claim 12 wherein said  
2 first row of adder cells contains  $N$  adder cells and said second row  
3 of adder cells preceding said first row contains less than  $N$  adder  
4 cells.

1 *Final* 23. A method of adding a first M-bit argument and a second M-  
2 bit argument in an M-bit adder, the M-bit adder comprising M adder  
3 cells arranged in R rows, the method comprising the steps of:

4 receiving a first data bit,  $A_x$ , from the first M-bit  
5 argument and a first data bit,  $B_x$ , from the second M-bit argument  
6 in a least significant adder cell in a first one of the rows of  
7 adder cells;

8 calculating in the least significant adder cell a first  
9 conditional carry-out bit,  $C_x(1)$ , assuming a row carry-out bit from  
10 a second row of adder cells preceding the first row is a 1;

11 calculating in the least significant adder cell a second  
12 conditional carry-out bit,  $C_x(0)$ , assuming the row carry-out bit  
13 from the second row is a 0;

14 calculating in the least significant adder cell a first  
15 conditional sum bit,  $S_x(1)$ , assuming the row carry-out bit from the  
16 second row is a 1;

17 calculating in the least significant adder cell a second  
18 conditional sum bit,  $S_x(0)$ , assuming the row carry-out bit from the  
19 second row is a 0;

20 propagating the  $C_x(1)$  bit and the  $C_x(0)$  bit to a second  
21 adder cell in the first row of adder cells; and

22 selecting one of the  $S_x(1)$  bit and the  $S_x(0)$  bit to be

23 output from the least significant adder cell according to a value  
24 of the row carry-out bit from the second row.